Attorney Docket No. YO999-369

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) Apparatus for use in summing at least two binary values, comprising:

a binary adder circuit, responsive to a first binary value, a second binary value and a carry value, and operative to generate a binary output signal S(n) representative of a summation of the first binary value, the second binary value and the carry value, the binary adder circuit having dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic logic, for implementing an exclusive OR function that generates the binary output value without one of a positive and a negative complementary version of the carry ~~value.~~ value;

wherein the binary output signal S(n) is implemented in accordance with an expression: ^(p(n) * C(n-1))*(p(n) + C(n-1)), where C(n-1) is a generate signal from a binary value n-1 associated with the carry value, p(n) is a propagate signal associated with the first binary value and the second binary value, ^ is a logical complement operator, * is an AND operator, and + is an OR operator.

2. (Canceled)

3. (Currently amended) The apparatus of claim ~~2~~ 1, wherein the logic of the binary adder circuit comprises:

a first NMOS transistor stage for performing an AND operation on the generate signal and the propagate signal;

an inverter stage, coupled to the first NMOS transistor stage, for inverting an output signal generated by the first NMOS transistor stage;

a second NMOS transistor stage for performing an OR operation on the generate signal and the propagate signal; and

a NOR gate, coupled to the inverter stage and the second NMOS transistor stage, for

combining an output signal generated by the inverter stage and an output signal generated by the second NMOS transistor stage to generate the binary output value.

4. (Original) The apparatus of claim 3, wherein the first NMOS transistor stage is responsive to more than one generate signal and more than one propagate signal.

5. (Original) The apparatus of claim 4, wherein the second NMOS transistor stage is responsive to more than one generate signal and more than one propagate signal.

6. (Currently amended) A dynamic N-bit parallel adder, comprising:

a first logic stage, the first logic stage configured to receive a first N-bit binary value and a second N-bit binary value and compute generate signals and propagate signals for each bit;

a second logic stage, coupled to the first logic stage, the second logic stage configured to compute block generate signals and block propagate signals for groups of one through m bits from the generate and propagate signals computed in the first logic stage;

a third logic stage, coupled to the second logic stage, the third logic stage configured to combine the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

a fourth logic stage, coupled to the third logic stage, the fourth logic stage configured to combine remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and to generate a summation signal wherein the summation signal represents the logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation;

wherein at least one of the logic stages has dynamic logic, without inversion of signals driving one or more dynamic nodes associated with the dynamic ~~logic.~~ logic; and

wherein the fourth logic stage implements an exclusive OR function to generate the summation signal and bit i of the summation signal is: $\overline{[p_i G_{i-1} + p_i P_{i-1} G_{i-2} + p_i P_{i-1} P_{i-2} G_{i-3}]}\,[G_{i-1} + P_{i-1} G_{i-2} + P_{i-1} P_{i-2} G_{i-3} + p_i]$, where p is a

propagate signal and g is a generate signal and P is a group propagate signal and G is a group generate signal.

7. (Previously presented) The parallel adder of claim 6, wherein a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i, wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$, where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i where a_i represents the first binary value and b_i represents the second binary value, and where p_i represents the propagate signal and is equivalent to a logical summation operation between a_i and b_i.

8. (Original) The parallel adder of claim 6, wherein the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals.

9. (Canceled)

10. (Canceled)

11. (Original) The parallel adder of claim 6, wherein N is equal to 64.

12. (Original) The parallel adder of claim 6, wherein the logic stages are implemented with complementary metal oxide semiconductor components.

13. (Currently amended) A method of adding, in parallel, a first N-bit binary value and a second N-bit binary value, the method comprising the steps of:

computing generate signals and propagate signals for each bit;

computing block generate signals and block propagate signals for groups of one through m bits from the generate and propagate signals computed in the first computing step;

combining the block generate and block propagate signals of one set of groups with the block generate and block propagate signals of another set of groups; and

combining remaining uncombined block generate and block propagate signals with a propagate signal associated with each bit, and generating a summation signal wherein the summation signal represents the dynamic logical addition of the first and second binary values and the summation signal is generated without a need for one of positive and negative complementary signal generation;

wherein the dynamic logical addition is performed without inversion of the generate signals, propagate signals, block generate signals and block propagate ~~signals.~~ signals; and

wherein the summation signal is generated in accordance with an exclusive OR function and bit i of the summation signal is $\overline{[p_iG_{i-1}+p_iP_{i-1}G_{i-2}+p_iP_{i-1}P_{i-2}G_{i-3}]}\,[G_{i-1}+P_{i-1}G_{i-2}+P_{i-1}P_{i-2}G_{i-3}+p_i]$, where p is a propagate signal and g is a generate signal and P is a group propagate signal and G is a group generate signal.

14. (Previously presented) The method of claim 13, wherein a generate signal and a propagate signal computed for a bit i in the first logic stage represent a carry signal c_i, wherein c_i is equivalent to $g_i + (p_i\ c_{i-1})$, where g_i represents the generate signal and is equivalent to a logical multiplication operation between a_i and b_i where a_i represents the first binary value and b_i represents the second binary value, and where p_i represents the propagate signal and is equivalent to a logical summation operation between a_i and b_i.

15. (Original) The method of claim 13, wherein the summation signal is generated without the use of one of positive and negative complementary generate and propagate signals.

16. (Canceled)

17. (Canceled)

18. (Previously presented) The method of claim 13, wherein N is equal to 64.

19. (Original) The method of claim 13, wherein the computing, combining and generating steps are implemented with complementary metal oxide semiconductor components.

20. (Canceled)